Chapter 10

Conclusions

This chapter presents an overview of the initial research into DSL simulator requirements, appropriate signal processing techniques, implementation options and two specific designs. Finally, a brief discussion of the simulator's extension to full and bandwidth limited VDSL systems is presented.

10.1 The Modelling Requirement

A simulator emulating a twisted copper access pair at DSL frequencies must adequately model the line's physical impairments of insertion loss and phase shift, and also the effects of noise and crosstalk from other access lines within the same bundle.

10.1.1 Physical Line Effects

Insertion loss and phase shift are functions of conductor diameter, access reach and frequency. Theoretical development of a line's attenuation and its effect on a signal's phase from the four primary line characteristics of inductance, capacitance, inductance and resistance lead to transfer function expressions for insertion loss and phase response or shift. Theoretical results closely match those experienced on real DSL lines and can be used as a basis for determining the physical line modelling requirements.

Over DMT ADSL bandwidths and reach, total insertion losses of upto 62 dB can be expected. For VDSL systems operating at upto 20 times the frequency, but at greatly reduced reaches, losses as high

as 120 dB occur. For a given length of twisted copper pair, the rate of change of insertion loss with frequency is greatest at lower frequencies. For example on a 6 kft 26 gauge PIC line, the insertion loss changes by 34 dB between DC and 1.25 MHz and by just 14 dB between 1.25 and 2.5 MHz (figure 4.1).

Unlike insertion loss, phase shift changes linearly with frequency (figure 4.3). Over even the shortest reach, the phase undergoes many rotations over both the ADSL and VDSL bandwidths. The full phase rotation bandwidth for short 1 kft lines is approximately 275 kHz and just 23 kHz for longer 12 kft pairs (table 4.3).

Although only a reproduction of material in chapter 3, the complex nature of the twisted copper pair's response over 10 MHz is shown below as its nature is crucial to the simulation signal processing approach taken.

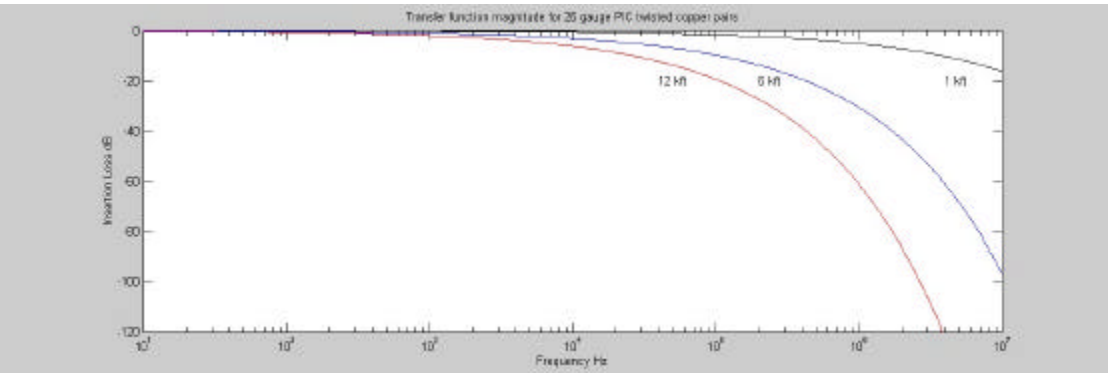

Figure 10.1 Insertion loss for 26 gauge PIC twisted copper pair

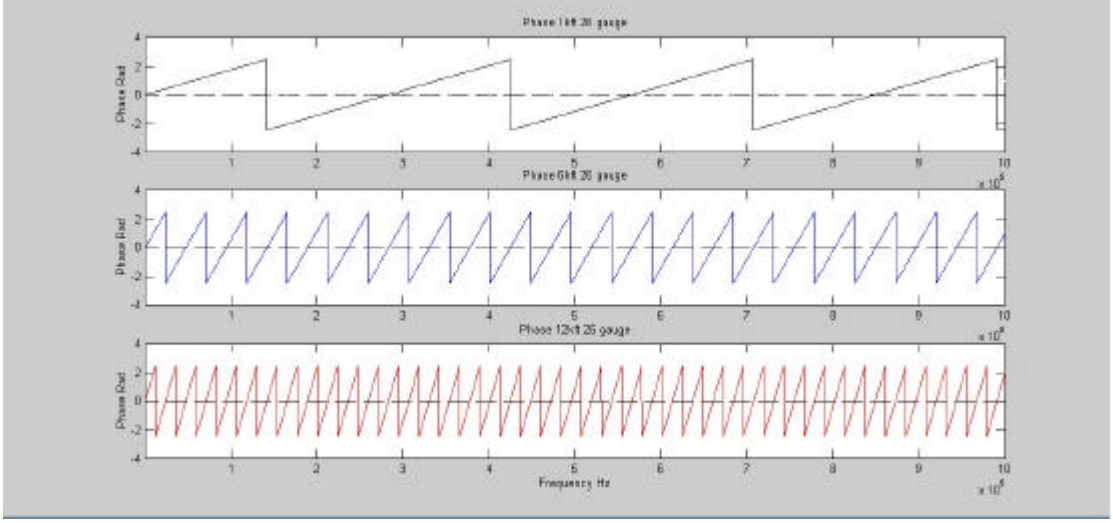

Figure 10.2 Phase shift for 26 gauge PIC twisted copper pair over ADSL bandwidth

10.1.2 Crosstalk and Noise

At extended DSL transmission frequencies, crosstalk from other access lines becomes significant. Crosstalk can be classified into two types: self and foreign. Self crosstalk is an induced signal from and disturber of the same access type whereas foreign crosstalk is due to a disturber of a different access type. For example, self ADSL crosstalk occurs between two ADSL lines within the same bundle whereas foreign crosstalk occurs between ADSL and ISDN lines.

DSL modem receivers incorporate sharp bandpass filtering, so in the absence of non-linear intermodulation distortion, only crosstalk within the DSL transmission bandwidth of the modem under test is significant because any out of band crosstalk is rejected by the receiver.

In addition to crosstalk type, the nature of its induction is also classified as Near End CrossTalk (NEXT) or Far End CrossTalk (FEXT). However, this is irrelevant to the line simulator hardware as NEXT and FEXT crosstalk incident on a receiver can't be distinguished (ignoring the case of 'self' induced self NEXT whereby a receiver could distinguish the difference because of the correlation between the signal it is transmitting and that which it is receiving due to crosstalk). Rather, the software to drive the hardware would take into account the nature of NEXT and FEXT in generating a realistic crosstalk model.

Both AGWN and coloured bandpass noise are incident on DSL lines. For the same reason as crosstalk, only noise occupying the relevant DSL spectrum need be simulated.

10.2 Signal Processing Methods

Signal modification in the frequency domain provides possibly the only method of simulating the physical line's response due to the tight control required over phase, shown in figure 10.2. The method of signal manipulation in the frequency domain, known as frequency domain filtering, has long been practised in the field of medical CT and MRI scanning where processing is non-real time. The principle of multiplying each DFT signal sample with a complex filter coefficient at that frequency is both simple to understand and elegant. The main reason for its limited use in the telecommunication's arena is the need to compute a frequency domain description of the signal using a DFT before any manipulation can take place and then to transform the result back to the time domain with an IDFT. Once time – frequency and the reverse transformations can be computed in real time (i.e. in the same time it takes to sample the N points of the transform, known as the time sampling window), frequency filtering offers a very powerful tool.

In addition to modelling the line's physical response, noise and crosstalk that are both fundamentally additive in nature, can be modelled in the frequency domain by the simple addition of complex components to each DFT sample.

Initially simulation by signal manipulation solely in the frequency domain was developed. However, some noise, especially impulsive noise is more readily described in the time domain through addition to time samples. The revised simulator design includes an additional time domain manipulation block.

Generation of crosstalk in a hybrid time and frequency domain simulator can be achieved by either the addition of suitable DSL line code time samples at the time manipulation stage or through the addition of suitably modified discretised PSD masks in the frequency domain. The latter method can be used to simply simulate self crosstalk through the addition of an attenuated and delayed copy of the actual ADSL signal from the modem under test. Foreign crosstalk can be simulated through the addition of the theoretical or measured PSD of a foreign disturbing signal, a simpler approach than the generation and addition of specific line codes in the time domain.

10.3 DFT Requirements

The requirements for the DFT used within the simulator consist of the maximum transform frequency resolution or cell size, the amplitude precision (i.e. quantisation interval) and the transform computation time for real time simulator operation.

The frequency transform resolution determines the accuracy to which the discrete model of the line and transmission process reflects the actual continuous line. For the physical line effects, an initial figure of a maximum 10% difference between the continuous line's response and the discrete model's constant response over any transform cell was considered.

DSL systems incorporate frequency division multiplexing to allow POTS to co-exist alongside data transmission at higher frequencies. This coupled with the strict bandpass filtering of the modem receivers, allows the line's behaviour at frequencies below the lowest frequency used by the DSL modulation scheme to be ignored. ADSL's FDM with the POTS is fortuitous as concerns the size of the required DFT, as the greatest variation of insertion loss occurs in the 30 kHz band reserved POTS (figure 4.1). VDSL's FDM is with both POTS and ADSL, allowing the spectral band from DC to about 1.2 MHz to be ignored. The FDM nature of DSL transmission gives rise to the concept of the first relevant transform interval for simulation as being the first DFT cell within the DSL PSD, not from DC (section 4.1.1 and table 4.2).

ADSL simulator systems require at least 256 transform cells over the 1.1 MHz bandwidth giving a maximum transform cell size of 4.3125 kHz due to insertion loss (table 4.2) and coincidentally the same considering phase shift (table 4.5, strictly for 6 kft lines only). VDSL systems with a greater bandwidth, but first relevant transform interval from just above the 1.1 MHz ADSL spectrum, require at least 741 transform cells over the 20 MHz transmission bandwidth.

In addition to the physical line effects, the DFT cell size's effect on crosstalk modelling must also be considered. For DMT systems, in order to model crosstalk and noise within a particular transmission bin, the discrete representation of the signal must have at least one sample across that bin's local bandwidth. ANSI DMT ADSL, the only developed or proposed DMT system, has 256 subcarriers

spaced at 4.3125 kHz, therefore the DFT employed must have at least 256 samples across the 1.1 MHz ADSL bandwidth and spaced at the 4.3125 kHz DMT frequencies. The same arguments don't apply to single 'carrier' CAP ADSL and CAP/QAM VDSL systems. In the absence of stricter needs, the insertion loss and phase shift requirements for ADSL were assumed sufficient to model crosstalk and noise for these other two systems. Overall, the most stringent requirement arising from insertion loss, phase shift and crosstalk modelling requirements must be implemented. For DMT ADSL systems, all three maximum transform cell requirements were equal at 4.3125 kHz.

In addition to the minimum Nyquist sampling rate of twice the required maximum observable frequency, sampling guard bands are required, thus increasing the necessary A/D conversion rate. For real time simulation, Fast Fourier Transforms are required. When radix 2 or 4 FFT algorithms are used and sufficient sampling guard bands included, the simulator transform parameters in table 10.1 result.

	Sampling Rate	Transform Size
DMT ADSL	4.416 MSPS	1024 point (radix 2 or 4)
CAP ADSL	4.416 MSPS	1024 point (radix 2 or 4)
VDSL	50 MSPS	2048 point (radix 2) 4098 point (radix 4)

Table 10.1 FFT Transform Parameters

Quantisation precision must be at least as good as that used in the modems attached to the simulator. A minimum of 15 to 16-bits is required.

10.4 Implementation Paths

Of the three methods of implementing the FFT and IFFT processes considered, DSPs and FPGAs were found viable. After extensive research into performance, ADSL simulation using either technology was thought to be possible. VDSL simulation is currently not feasible without extensive parallel processing techniques. Implementation with DSPs is possibly the most versatile interms of the ease of functional evolution without hardware redesign and extension to VDSL simulation. However, the development and production costs and suitability of development within the university environment favour the FPGA implementation route.

FFT modules for both solutions exist in the form of software code for DSP platforms and Reference logic designs for FPGAs, avoiding the need for complex and time consuming customised transform engine design.

10.5 ADSL Line Simulation Using FPGAs

A simulator board based around Xilinx FPGAs using the FFT Reference Design to provide both the FFT and IFFT functions and with separate time and frequency manipulation blocks requires three separate FPGA processing devices. With three FPGAs, sufficient unused logic capacity exists to implement all necessary memory addressing, read / write and control strobing, memory interface paging and local and global clock circuitry. Dual port RAM memory interfaces between each functional block allows both independent operation within the confines of each time sampling window limit and a pipelined block processing approach. Designing individual blocks is greatly simplified by this timing independence, as internal timing considerations are local to the individual operations themselves. In addition, although there is a question mark over the validity of the results produced by the FFT Reference Design, different replacement FFT and IFFT engines can easily be used in the modular design with memory interfacing. The use of ADCs and DACs within ADSL AFEs simplifies the analogue and conversion side of the design.

Functionality testing of the manipulation blocks confirmed arithmetic operation and process execution times within the 232 μs time sampling window. Functionality testing of the FFT Reference design resulted in an invalid result for a real valued odd sampled sinusoidal input vector. Timing analysis confirmed the transformation process is also completed well within the sample window limit.

Each transform block fits into XC4062XLA-07HQ240 FPGAs with all manipulation circuitry into the smaller XC4013XLA-07HQ240 FPGA. Chip costs are £498 for the two XC4062XLA devices and £60 for the XC4013XLA from MicroCall Ltd.

10.6 Further Work

The major question remaining before a prototype ADSL simulator can be built is whether the FFT engine does indeed produce invalid results. The use of ready made Xilinx FFT designs has been problematic to say the least and it is difficult to see how extensive testing can be carried out on the transform operation because of the lack of a complete, ‘clean’ FFT module that includes the necessary scratchpad RAM to simulate within the Foundation environment. However, if the new Virtex targeted FFT materialises and includes behavioural models, this is probably the best path to follow as it is doubtful whether much support for the XC4000 FFT Reference Design can be gained.

If neither the current FFT Reference Design or new Virtex design proves suitable, there is always the possibility of designing a purpose built transform engine.

In addition to finalising the FFT engines, the PC interface needs to be developed and well documented to allow separate development of the associated hardware. The software driver for the board needs to be written, a major task requiring close collaboration with companies developing new modems to determine the required simulation functionality. An accurate line simulation through appropriate

multiplication and addition vectors for the physical line, crosstalk and noise, will require access to a physical access line for experimental test measurements.

10.7 Towards a VDSL Line Simulator

The main hurdle to an economically viable solution to VDSL line simulation is speed of FFT / IFFT processing. Without an approximate trebling of DSP processing speed or ten-fold increase in FPGA speeds, currently the only method of implementing the simulator would be to use FFT processes which take several time sampling windows to compute, and have several FFT engines working on subsequent separate windows of data concurrently. In this way, if the FFT took say four sample windows to complete, a total of four processing engines would be required. This is perhaps not surprising when one considers that although DMT is by far the more versatile modulation scheme compared to QAM / CAP, signal processing has only recently reached the level where DMT functionality can be viably incorporated into consumer electronic ADSL modems.

Towards the end of the project some discussion with Fujitsu brought forward the idea of a limited bandwidth VDSL simulator. Tentative figures for modems operating upto frequencies of the order of 5 to 6 MHz at 1 kft were suggested. Sampling at 13 MSPS (6 MHz observable spectrum with a 0.5 Mhz guard band), a 1024 sample window is 79 µs long. If the FFT Reference design is found to be correct, targeted at the fastest XLA device, FFT processing times of 75 µs are predicted by the Foundation place and route software, clearly such a simulator is feasible now.